

### 16 PIN, 5 TAP, ECL ACTIVES

DC Electrical Characteristics					
Parameter	*Test Conditions	Min	Max	Unit	
$V_{OH}$	High Level Output Voltage	$V_{IL} = \text{Min}$	-960		mV
$V_{OHT}$	High Level Output Threshold Voltage		-980		mV
$V_{OLT}$	Low Level Output Threshold Voltage		-1630		mV
$V_{OL}$	Low Level Output Voltage	$V_{IH} = \text{MAX}$	-1650		mV
$I_{IH}$	High Level Input Current	$V_{IH} = \text{Max}$	265	uA	
$I_{IL}$	Low Level Input Current	$V_{IL} = \text{Min}$	0.5		uA
$I_{EE}$	Supply Current		50		mA

\* ( $V_{CC1} = V_{CC2} = \text{GND}$ ,  $V_{EE} = 5.2\text{V} \pm 0.01\text{V}$ , Output Loading with  $50\Omega$  to  $-2.0\text{V} \pm 0.01\text{V}$ )

Recommended Operating Conditions				
Parameter	Min	Max	Unit	
$V_{EE}$	Supply Voltage (Negative)	4.94	5.46	V
$V_{CC}$	Circuit Ground (Pins 1 and 16)	0	0	V
$V_{IH}$	High Level input Voltage	-980	-810	mV
$V_{IHT}$	High Level Input Threshold Voltage	-1105		mV
$V_{IL}$	Low Level input Voltage	-1850	-1630	mV
$V_{ILT}$	Low Level Input Threshold Voltage		-1475	mV
$P_W$	Pulse Width % of Total Delay	40		%
$T_A$	Operating Free-Air Temperature	-30	+80	°C

Input Pulse Test Conditions @ 25°C			Unit
$V_{IN}$	Pulse Input Voltage	-1.0V (-0.75 to 1.75V)	
$P_W$	Pulse Width	3 x Max Delay	
$T_{RI}$	Pulse Rise Time(20% to 80%)	2 nS	
$P_{RR}$	Pulse	10 x $T_d$	
$V_{EE}$	Supply Voltage	-5.2V	

TAP 1	TAP 2	TAP 3	TAP 4	OUTPUT	RISE TIME	POLARA P/N
nS ± 5%	nS MAX	AWK - PINOUT				
3.0 TYP*	4 ± 0.5	5 ± 0.5	6 ± 0.5	7 ± 0.5	4	AWK-0007
3.0 TYP*	5 ± 0.5	7 ± 0.5	9 ± 0.5	11 ± 0.5	4	AWK-0011
3.0 TYP*	6 ± 0.5	9 ± 0.5	12 ± 1.0	15 ± 1.5	4	AWK-0015
4 ± 1.0	8 ± 0.5	12 ± 1.0	16 ± 1.5	20 ± 2.0	4	AWK-0020
5 ± 1.0	10 ± 1.0	15 ± 1.5	20 ± 2.0	25 ± 2.0	4	AWK-0025
6 ± 1.0	12 ± 1.0	18 ± 1.5	24 ± 2.0	30 ± 2.0	4	AWK-0030
8 ± 1.0	16 ± 1.5	24 ± 2.0	32 ± 2.0	40	5	AWK-0040
10 ± 1.0	20 ± 2.0	30 ± 2.0	40	50	5	AWK-0050
15 ± 1.5	30 ± 2.0	45	60	75	8	AWK-0075
20 ± 2.0	40	60	80	100	10	AWK-0100
30 ± 2.0	60	90	120	150	15	AWK-0150
40	80	120	160	200	20	AWK-0200
50	100	150	200	250	25	AWK-0250
60	120	180	240	300	30	AWK-0300
70	140	210	280	350	35	AWK-0350
80	160	240	320	400	40	AWK-0400
90	180	270	360	450	45	AWK-0450
100	200	300	400	500	50	AWK-0500

Delay Time measured at -1.3V, no load

Delay Times referenced from Input to Leading Edges

\* Inherent Delay

Rise Time measured from 20% to 80%

Output terminated (externally) with  $50\Omega$  to -2.0VDC

